

**REMARKS**

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for careful consideration of this application.

**Disposition of Claims**

Claims 1-8 were pending in this application. Claim 6 has been canceled by way of this reply. Therefore, claims 1-5 and 7-8 are currently pending. Claims 1, 2, 5, and 7-8 are independent. The remaining claims depend, either directly or indirectly, from claim 2. Claims 1-5 have been withdrawn from consideration.

**Claim Amendments**

Claim 6 has been canceled by way of this reply. The subject matter of claim 6 has been incorporated into claims 7 and 8, respectively. Support for these amendments can be found, for example, in claim 6 as filed. No new matter has been added by these amendments.

**Rejections under 35 U.S.C. § 102**

Claim 6 stands rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 2003/0001254 ("Jackson"). Claim 6 has been canceled by this reply, rendering this rejection moot with respect to the claim. Accordingly, withdrawal of this rejection is respectfully requested.

**Rejections under 35 U.S.C. § 103***Claim 6*

Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable in view of Jackson. Claim 6 has been canceled by this reply, rendering this rejection moot with respect to the claim. Accordingly, withdrawal of this rejection is respectfully requested.

*Claim 7*

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable in view of Jackson. This rejection is respectfully traversed.

As is well-known to those of ordinary skill in the art to which the claimed invention pertains, methods for mounting and packaging an IC on a PCB can be categorized generally into the Pin Grid Array (the PGA) and the Ball Grid Array (the BGA). The PGA is a package with one face covered (or partly covered) with pins in a grid pattern. These pins are used to conduct electrical signals and power between the IC and the PCB it is placed on. In contrast, for a BGA type IC, pins are replaced by balls of solder attached to the bottom of the package. The BGA type IC is placed on a PCB that carries copper pads in a pattern that matches the solder balls, and the solder balls in place of pins conduct electrical signals and power between the IC and the PCB. This classification is described in Jackson as well (*see* Jackson, paragraph [0003]).

The invention as recited in claim 7 is directed to a mounting structure of *a ball grid array type IC*. Because claim 7 recites *the ball grid array type IC*, it is clear to one of ordinary skill in the art that the pins except for the solder balls do not conduct signals and power

between the board and the body portion of the ball grid array type IC. Specifically, independent claim 7, as amended, requires, in part, mounting *the ball grid array type IC* on a board.

In contrast, Jackson is directed to packaging an IC by using both types of arrays, i.e., the PGA and BGA. Jackson intends to increase the total power capacity of pins to a desired value by using multiple pins (i.e., the PGA) whereas solder balls conduct signals between upper and lower substrates (i.e., the BGA).

For a better understanding, referring to Figure 1D and paragraph [0017], Jackson describes that the pins 110 are electrically connected to the holes 102 and, thus, provide power connections 122 between the first and second substrates while the solder balls 114 provide signal connections 120. Jackson mentions this configuration and the advantages associated therewith numerous in the disclosure (*see, e.g.,* paragraphs [0018], [0020], and [0022]).

That is, Jackson is contrary to a mounting structure of a ball grid array type IC as recited in independent claim 7 and, therefore, fails to disclose mounting *the ball grid array type IC* on a board, as required by claim 7.

Moreover, independent claim 7, as amended, further requires, in part, *the anti-rubbing pin provided on each of three corners of the body portion* so as to protrude downward.

In one embodiment according to the claimed invention, as shown in Figures 5A and 5B, by providing anti-rubbing pins on three corners of a body portion of a ball grid array type IC, the orienting and positioning work of the IC can be performed more efficiently because these three anti-rubbing pins can define a single position/orientation of the IC on a board.

In contrast, Jackson is completely silent with respect to such pin arrangement of claim 7. Referring to Figures 1A-1B of Jackson, it is noted that Jackson contemplates only a

mounting structure which has pins 110 arranged symmetrically. If a mounting structure has pins arranged in (diagonally or foldedly) symmetrical positions, it can not define a single position/orientation of an IC on a board (*see*, e.g., Figures 4A and 4B of the present application). That is, the mounting structure of Jackson can not define a single position/orientation of an IC on a board because of its symmetrical nature.

In view of the above, Jackson does not teach or suggest *the anti-rubbing pin provided on each of three corners of the body portion* so as to protrude downward, as required by claim 7. In addition, as discussed above, Jackson does not teach or suggest mounting *the ball grid array type IC* on a board, as required by claim 7. Because Jackson does not teach or suggest each and every limitation of amended claim 7, claim 7 is patentable. Accordingly, withdrawal of this rejection is respectfully requested.

#### Claim 8

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable in view of Jackson. This rejection is respectfully traversed.

As in claim 7, independent claim 8, as amended, requires, in part, mounting *the ball grid array type IC* on a board. As set forth above, Jackson fails to disclose mounting *the ball grid array type IC* on a board, as also required by claim 8.

Moreover, independent claim 8, as amended, further requires, in part, a pin which is shaped like *a square in section* to be inserted into a square hole in the board is provided on another corner of the bottom surface of the body portion diagonally opposite the anti-rubbing pin.

In one embodiment according to the claimed invention, as shown in Figure 6, by providing another pin in a square shape at the opposite corner to an anti-rubbing pin, the orienting and positioning work of the IC can be performed more efficiently because the pin in a

square shape and the anti-rubbing pin can define a single position/orientation of the IC on a board.

In contrast, Jackson is completely silent with respect to such pin arrangement of claim 8. As discussed above, the mounting structure of Jackson having pins in symmetrical positions can not define a single position/orientation of an IC on a board.

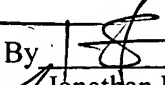
In view of the above, Jackson does not teach or suggest a pin which is shaped like *a square in section* to be inserted into a square hole in the board is provided on another corner of the bottom surface of the body portion diagonally opposite the anti-rubbing pin, as required by claim 8. In addition, as set forth above, Jackson does not teach or suggest mounting *the ball grid array type IC* on a board, as required by claim 8. Because Jackson does not teach or suggest each and every limitation of amended claim 8, claim 8 is patentable. Accordingly, withdrawal of this rejection is respectfully requested.

**Conclusion**

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 04995/132001).

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Respectfully submitted,

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